

Average and Static Power Analysis of a 6T and 7T SRAM Bit-Cell at 180nm, 90nm, and 45nm CMOS Technology for a High Speed SRAMs

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Abstract- A lot of consideration has been given to problems arising due to power dissipation. Different ideas have been proposed by many researchers from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between the power, delay and area. This is why; the designers are required to choose appropriate techniques that satisfy application and product needs. Another important component of power which contributes to power dissipation is Dynamic Power. This power is increasing due to prolonged use of the electronic equipments. This is due to the fact that now-a-days people are working on electronic systems from morning till night; it may be a mobile phone or a laptop or any other equipment. This paper deals with the estimation of two components of power i.e. static power (when device is in the standby mode) and the average power (average amount of energy consumed with respect to time) of a 6T and 7T SRAM (Static Random Access Memory) bit-cell at 180nm, 90nm, and 45nm CMOS Technology. This is done in order to estimate the power required for a high speed operation of 6T and 7T SRAM bit-cell.

Index Terms— Average power, dynamic power, static power, read power, write power, stability.

I. INTRODUCTION

In recent years, static random access memory (SRAM) has become the most widely used embedded memory which typically occupies the largest portion of SoC (System-on-chip) die area, and often dominates the total chip power. The power alone has a number of components which contribute to the leakage power. These are static power, dynamic power, and average power. Dynamic power further has components such as switching power, power due to glitches, short-circuit power. Till now emphasis has been given to static power, but in today's scenario dynamic power is also creating an issue. This power is increasing due to prolonged use of the electronic equipments which is due to the fact that now-a-days people are completely technology dependent; it may be a mobile phone or a laptop or a washing machine or any other equipment. In the past few years, tremendous rise in VLSI fabrication has led to increased densities of integrated circuits by decreasing the device geometries. Such high density circuits support high design complexities and very high speed, but they are susceptible to power consumption. Circuits with excessive power dissipation are more susceptible to runtime failures and give rise to reliability problems. A lot of research is being done to resolve electrical parameter. The CTs and PTs used for protection are sufficient for measuring these electrical parameters. the issue of power leakage, but each time a new method is evolved; it throws its impact on the

other parameters of the device. This paper analyses the two components of power i.e. average and static power of 6T and 7T SRAM bit-cells. It also discusses the functional view and a review of a 6T and 7T SRAM bit-cells respectively.

II. CONVENTIONAL 6T SRAM: A FUNCTIONAL VIEW

A conventional 6T SRAM comprises of 6 transistors designed simply to form two cross coupled inverters placed back-to-back. This cell is used to either store a single bit data or read a single-bit data from the cell. When a bit is stored, the SRAM works as a latch. The small leakage currents of both the CMOS inverters contribute towards the total leakage power consumption of the memory cell. The use of cross coupled inverters leads to a slightly larger area consumption; which is a drawback as compared to the resistive load and depletion load NMOS SRAM Cell. The memory cell consists of a simple CMOS latch in which two inverters connected back-to-back and two complementary access transistors M1 and M2. As long as the power supply is available, the cell will preserve one of its two possible states. Conventional SRAM cell with 6T is shown in figure 1. There are mainly three states in SRAM cell the write, read and hold states. In the following paragraphs, we describe the states a conventional 6T SRAM cell:

A. Data Hold State

When $WL = "0"$, M1 and M2 disconnect the cell from bit lines (Bit and Bit bar). The current drawn in this state from the V_{dd} is termed as leakage current.

B. Data Read State

Read operation starts with pre-charging Bit and Bit bar to high. Within the memory cell M3 and M6 are ON. Asserting the word line, turns ON the M1 and M2 and the values of Q and Q' are transferred to bit-Lines. No current flows through M2, thus M2 and M6 pull Bit bar up to V_{dd} , i.e., Bit bar = "1" and Bit line discharges through M1 and M3. This voltage difference is sensed and amplified to logic levels by sense amplifiers [1].

C. Data Write State

The value to be written is applied to the bit lines and keep $WL="1"$. Thus to write data "0", we assert Bit=0, Bit bar="1" and to write data "1", the Bit = "1", Bit bar ="0".

III. 7T SRAM BIT-CELL: A REVIEW

In [2], a low overhead read/write assist circuitry is being proposed, which uses an additional transistor along with a floating ground as well as shown in figure 2. As a consequence, they have improved the write speed (31%), write power (31%), decreased read power (60%) and reduced the total average power consumption (44%). The trade-off lies in consuming a larger area. Mr. Naagesh S. Bhatt has presented a design which reduced the read delay as well as the write power dissipation at 32nm technology on H-Spice using CNTFET (carbon nano-tube field effect transistor) as the channel material instead of the usual bulk silicon in the traditional MOSFET structure[3]. In [4] distinct lines for read and write on 90 nm technology and below using cadence tool which in turn, improved the read SNM and write SNM by 22.5% and 21.1% respectively at a supply voltage of lesser than 0.7 V. A larger chip area was a trade-off. Characterization and simulation of different 7T SRAM topologies using Cadence tool at 45 nm technology has been discussed in [1]. It has been concluded that the power dissipation and the leakage power varies with the topology used whereas the timing behaviour remains the same. Static power dissipation and the increased area are the challenging issues. Emphasis on the impact of process, voltage and temperature variation of 6T and 7T SRAM cell at sub-45 nm technology using H-Spice have been done by Aminul Islam and Mohd. Hassan [5]. The read and write power are saved by 65.6% and 89% respectively. Dual-ended write and single-ended read operation ensures high read static noise margin of SRAM bit-cell without the expense of writability which is the point of discussion of this paper [6]. This paper has reduced the bit cell area as well as calculated the value of power consumed. This paper [7] has analyzed the power of an SRAM memory cell using Tanner tool at 130nm technology. It proposes that the delay in case of writing a '0' is 29% faster than the conventional SRAM. Average power to write a '0' has been reduced by 16% and power dissipation to write a '1' has been reduced by 54%. The trade off lies in larger area consumption as it includes one extra transistor that controls the overall capacitances during the write and read operation. Stability and SNM has been analyzed on Cadence Tool at 45 nm technology. It has been observed that the changes in SNM affect the stability of the cell [8].

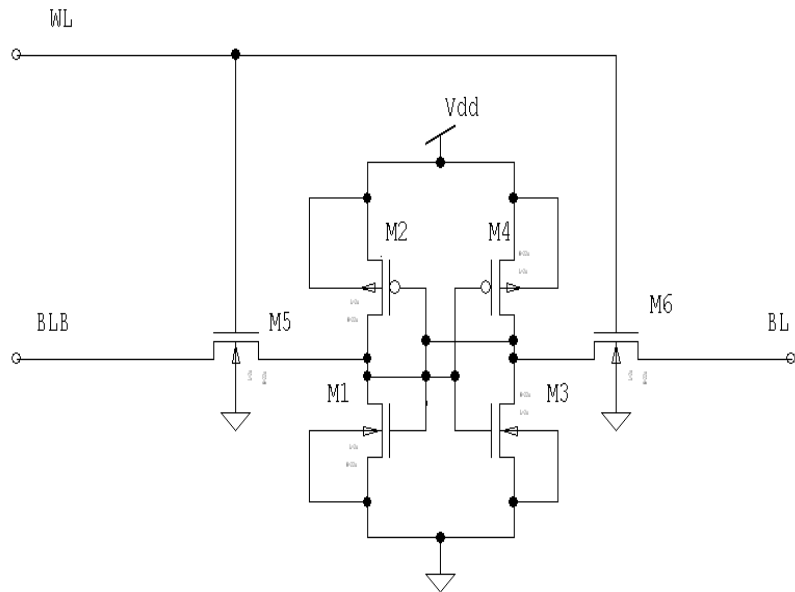


Figure 1. Conventional 6T SRAM Bit-Cell

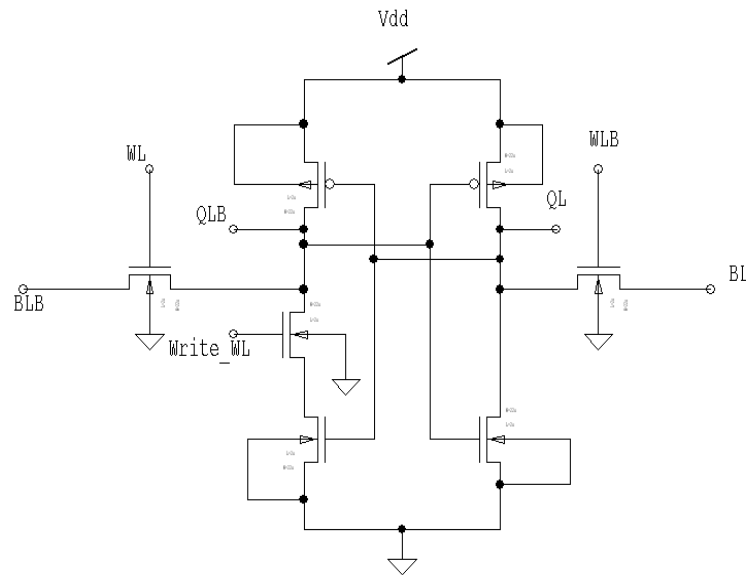


Figure 2. The 7T SRAM Bit-Cell

VI. CONCLUSIONS

The power consumption decreases as we move down to the lower sub-micron technologies. Figure 3 to figure 8 shows the simulation results and it has been seen that the conventional 6T SRAM bit-cell consumes more power in the static mode as compared to that in the dynamic mode. To overcome this, a 7T SRAM configuration was suggested which consumed lesser power in its static mode. This is due to an extra series nmos transistor, which led to the reduction in the static power of the device. Although the structure is more

stable, the area and the asymmetric configuration still remains a trade-off. The suggested configuration is best suited for applications that require the device to remain in the static mode for a larger duration of time.

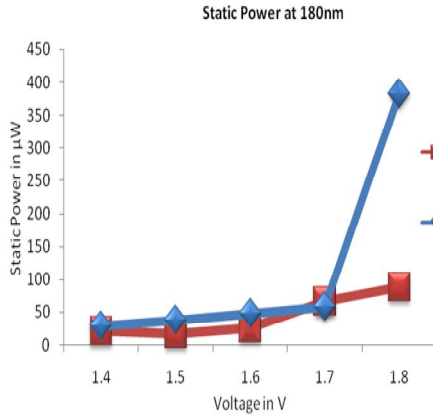


Figure 3. Static Power at 180nm

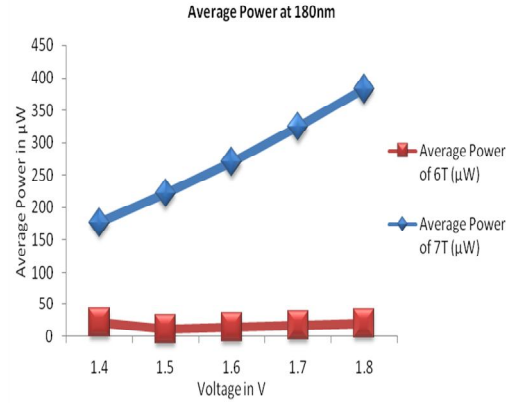


Figure 4. Average Power at 180nm

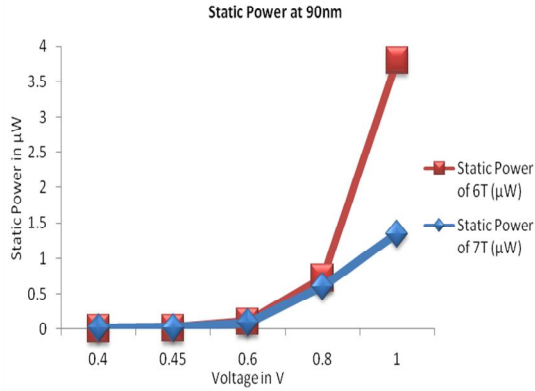


Figure 5. Static Power at 90nm

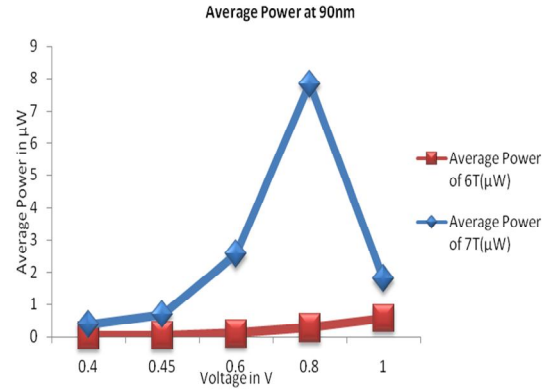


Figure 6. Average Power at 90nm

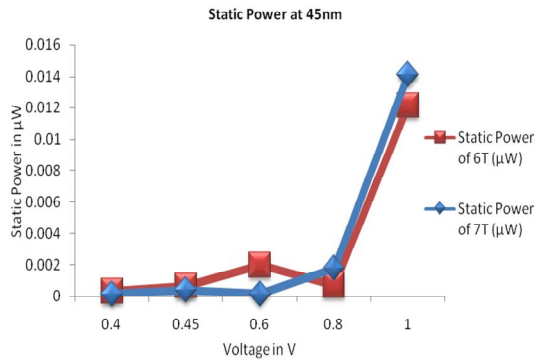


Figure 7. Static Power at 45nm

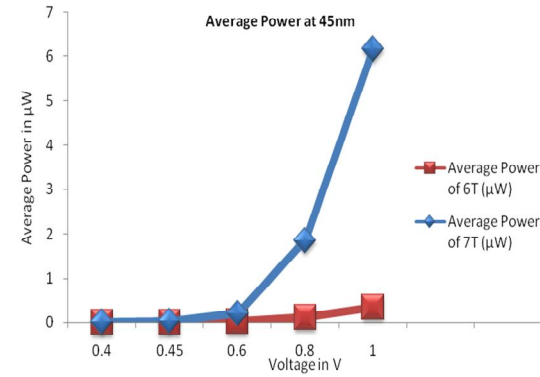


Figure 8. Average Power at 45nm

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